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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,134	09/24/2003	Andrew B. Kahng	0321.68261	2537

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,134	KAHNG ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 9-24* is/are rejected.

7)☒ Claim(s) *3-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 33 is objected to because of the following informalities:

Claim 11, line 2, delete "a least", insert – at least --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Aji et al. (US Pub. No.: 20040044979).

As to claims 1 and 23 Aji discloses:

(1) A method for evaluating a floorplan and for defining a global buffered routing for an integrated circuit, the method comprising the steps of:

constructing a graphical representation of the integrated circuit floorplan, including wire capacity (capacitance, delay, congestion, number of interconnect lines/number of routing tracks available through a gtile) and buffer capacity (number of repeaters, latches, cells have been inserted/added to satisfy constraints/limits that are

specified for a maximum transition time or maximum delay allowed) ([0008]; [0046];[0057];[0059];[0064]- [0065]; [0140];[0143]);

formulating an integer linear program from said graphical representation (By using an objective function that is a linear function of the number of solutions for each net, the optimization problem is formulated as a 0-1 integer programming problem) ([0048];[0155]); and

finding a solution to said integer linear program ([0156]-[0173]);

(23) A method for evaluating a floorplan and for defining a global buffered routing for an integrated circuit, the method comprising the steps of:

constructing a graphical representation of the integrated circuit floorplan, said constructing including ([0008]; [0046];[0057];[0059];[0064]- [0065]; [0143])

constructing a tile graph from the integrated circuit floorplan ([0060]-[0064]),

formulating a floorplan evaluation problem from said tile graph ([0049]; [0140]), and

constructing a gadget graph (partition intersection graph) from said tile graph ([0049]; [0141]-[0154]);

formulating said floorplan evaluation problem as an integer linear program from said graphical representation(By using an objective function that is a linear function of the number of solutions for each net, the optimization problem is formulated as a 0-1 integer programming problem) ([0048];[0155]); and

finding a solution to said integer linear program, said finding including finding a solution to a fractional relaxation of said integer linear program ([0156]-[0173]), and

rounding said solution to said fractional relaxation to an integer solution using randomized rounding ([0156]-([0157]).

As to claims 2, 9-22 and 24 Aji recites:

(2) The method recited in claim 1, wherein

said constructing said graphical representation includes constructing a tile (gtile) graph G from the integrated circuit floorplan, said tile graph G including ([0060]-[0064])

V, a sei of tiles v that represents the IC floorplan ([0047]);

E, a setof two-dirnensional edges between any two of said tiles v that are contiguous ([0061]);

B(v), a set of buffer capacities, each of said buffer capacities being a number of buffer sites located in each of said tiles v ([0057]; [0059]);

w(e), a set of wire capacities, each of said wire capacities being a number of wire routing channels (number of routing tracks available through a gtile) across each of said edges e ([0065]); and

a netlist set N of nets Ni such that N = {N1, N2, ..., Nk} to be included in the floorplan, each of said nets Ni specified by sets of source tiles Si, said source tiles Si being tiles v to which ad least one net source si may be assigned and by sets of sink tiles Ti, said sink tiles Ti being tiles v to which at least one net sink ti may be assigned ([0065]-[0066]);

(9), (10) The method, further comprising: evaluating routing and buffer resources using said solution, wherein said evaluating includes computing a tradeoff curve for a total routing area, a wire congestion, and a buffer congestion ([0156]; claim18);

(11), (12) The method, further comprising: defining a least one feasible buffered routing using said solution by randomly choosing a path from arnong a plurality of paths yielded by said solution ([0169]-[0173]; claim 15);

(13)-(17) The method, wherein said graphical representation includes a representation of a flexibility for assignment of pins in the floorplan, polarity constraints associated with inverting buffers, a plurality of buffer sizes, a plurality of wire sizes, delay constraints ([0046]; [0057]- [0058]);

(18)-(19) The method, wherein said finding a solution to said integer linear program includes finding a solution for at least one net with a single source and a single sink (claim 15);

(20) The method recited in claim 1, wherein constructing said graphical representation includes constructing a tile graph having tiles of a plurality of sizes ([0150]);

(21) The method recited in claim 1, wherein said graphical representation includes a representation on constraints of buffers in specified sets of tiles ([0064]);

(22), (24) A computer-readable medium having computer-readable instructions for performing the method recited in claims 1 and 23 ([0180]).

Allowable Subject Matter

3. Claims 3-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A method for evaluating a floorplan and for defining a global buffered routing for an integrated circuit as recited in claim 1, wherein said constructing of graphical representation further includes a buffer congestion upper-bound of $\mu o \leq 0$; a wire congestion upper-bound of $vo \leq 0$; a length along said path Pi between tile vo and a first buffer in Bi has at most said wireload upper-bound U; a length between consecutive buffers in Bi has at most said wireload upper-bound U; a length between a last buffer in Bi and tile vli has at most said wireload upper-bound U; wherein each of said feasible buffered routings (Pi, Bi) has a relative buffer congestion of $\mu \leq \mu o$; and has a relative wire congestion of $v \leq vo$.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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